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Review—Semiconductor Integrated Radar for Sensing Applications

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This paper reviews recent developments of semiconductor integrated radar for modern sensing applications. It focuses on a few representative works of integrated radar sensor chips that operate in the continuous-wave mode and the ultra-wideband pulse mode. The benefits of solid state science and technology to modern radar-on-chip solution are clearly demonstrated through those examples. The paper also presents some commercial application case studies, and discusses the outlook of integrated radar solution and the corresponding need from future semiconductor technologies.

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The term “RADAR” was coined in the 1940s as an acronym for Radio Detection And Ranging or Radio Direction And Ranging.^{1,2} It refers to a system that uses radio waves to determine information of a target such as its velocity, range, direction (angle of signal arrival), and vibration of objects. Radar can be used to detect a large variety of objects ranging from clouds, terrains, oil/water surfaces, ships, aircrafts, motor vehicles, missiles, human subjects, animals, hand gestures, tennis ball, to micro-structures.

At its inauguration, Radar was developed mainly for military purposes. Because the information obtained from radar can illustrate the position of the object, radar systems have high military values by providing warning against intruding enemies and locating air, ground and sea targets. This gradually evolved into civilian applications for use on aircrafts, ships, roads, and in meteorology. For example, aviation radars provide aircraft information of other obstacles and weather around the flying path, and give accurate altitude readings. Marine radars monitor ships to prevent collisions and to assist navigation. Weather radars are commonly used to detect precipitation and wind, and are important for monitoring severe weather conditions such as tornadoes, thunderstorms, and winter storms. On the road, police officers use radar to detect the speed of vehicles.

A radar system usually consists of a transmitter circuitry producing high-frequency signals, a transmitting antenna sending the signals toward the target, a receiving antenna capturing the signal reflected from the target, and a receiver circuitry to extract the information of interest from the received signal. Traditionally, radar systems are bulky and expensive partially because of the cost in generating high-power signals to be transmitted toward a far-away target. A key component in radar systems used to be the cavity magnetron,³ which made it possible to mount radar systems on aircraft and ships for many practical military and navigation applications. However, magnetron is still not a minimized solution, and it adds payload to the power supply of the system. Besides the challenge of the microwave components in a radar system, signal processing was another reason that made it difficult for radar technology to be adopted in consumer electronic devices and applications. The detection mechanism frequently involves algorithms such as fast Fourier transform, matched filter, and autocorrelation, which used to be demanding tasks for low-cost hand-held devices and requires large computers.

As semiconductor technologies advanced rapidly in recent decades, an evolution has taken place in the radar community and drastically changed the concept of radar. The modern radar systems become highly integrated to serve for a multitude of consumer applications. Most of today’s semiconductor integrated radars have the key circuitry integrated on a single chip or a small printed circuit board. Although they have a small feature size, the densely deployed RF/millimeter-wave/analog signal conditioning circuits enable adaptive configuration of the radar beam direction, signal amplitude, and receiver sensitivity. Driven by sophisticated embedded signal processing and control circuits, they serve for highly diverse applications in our daily life. For example, integrated radar systems are used to detect human physiological movements and obtain long-term breathing pattern for sleep monitoring.^{4,5} They are also used to monitor the heartbeat of lab mice⁶ and cows in dairy farms.⁷ As a non-contact tool for human-computer interface, millimeter-wave radar chip sets can recognize hand and finger gestures in real time.⁸ Low-profile low-cost radars are widely installed for automatic door opening, light activation, intruder sensing, and smart utility controls.⁹ In addition, they are deployed along large structures such as bridges for structural health monitoring by detecting the vibration and deflection.¹⁰ Most recently, highly-integrated radar sensors are inserted as a key component in a sensor fusion package as the platform technology for self-driving cars. Researchers are also investigating modern radar with ultra-high resolution and powerful beamforming capability as an advanced imaging tool to overcome the signal attenuation problem of optical imaging technologies in complex environment.

Radars can be generally divided into two categories based on the format of the transmitted signals: continuous-wave (CW) radar and pulse radar. The CW radar has many sub-categories, such as the single-tone CW radar that operates in the Doppler¹¹ or interferometry mode, the frequency-modulated CW (FMCW) radar that sends out a chirp signal with a frequency dynamically changing in time domain, and the frequency shift keying (FSK) radar which switches back and forth among different transmit frequencies. Each category of radars has its specific advantages for certain purposes. The single-tone CW radar has a simple architecture that allows high-level system-on-chip integration. It pertains high accuracy in speed and relative displacement measurement, but does not measure the absolute distance between the radar and the subject (i.e., the “range” information). The FMCW radar is more powerful as it detects the absolute range of a target,¹² which

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Figure 1. One of the earliest continuous-wave radar sensor chips developed in the Bell Labs. [2007] IEEE. Reprinted, with permission, from Ref. 19.

can be used to further derive other parameters including speed and displacement. The FSK radar provides range information with certain limitations such as the range ambiguity, but occupies a smaller bandwidth than the FMCW radar. The pulse radar, which is sometimes labeled with ‘ultra-wideband’ (UWB) characteristics, has high spatial resolution due to its large-bandwidth nature and may be realized with a simple hardware architecture.¹³ Enabled by advanced semiconductor technology and embedded signal processing, a radar with multi-mode operation that involves several fundamental modes is also possible.¹⁴

This paper reviews recent developments of semiconductor integrated radar for modern sensing applications. The next two sections will focus on a few representative works of integrated radar sensor chips that operate in the CW mode and the UWB pulse mode, respectively. The benefits of solid state science and technology to modern radar-on-chip solution will be clearly demonstrated through those examples. Then, some commercial application case studies will be presented. Finally, the outlook of integrated radar solution and the corresponding need from future semiconductor technologies will be discussed.

Continuous-Wave Radar Sensor Chips

Integrated CW radar sensor chips.—One of the earliest integrated CW radar sensor chip was developed by researchers in Bell Labs with a direct-conversion quadrature receiver architecture. The RF front-end was integrated in both CMOS and BiCMOS technologies.^{15–18} Fig. 1 shows the chip implemented in 0.25- μm CMOS process and enclosed by an Amkor TQFP 48-pin package. The chip occupies an area of 4.2 mm $\times$ 4.0 mm. It delivered 3 dBm RF output power at 2.4 GHz, and dissipated 180 mW from DC supply.¹⁸ With the CMOS implementation, breathing and heartrate of a human subject were measured at 50 cm, and an 83% accuracy was reported. The

first generation of radar sensor chips operated with 1.6- and 2.4- GHz carrier frequencies. The 2.4 GHz radar used a quadrature receiver to avoid the null point problem in motion sensing detection,¹⁵ which happens when the mixer local oscillator signal and the received signal are either in-phase or 180° out-of-phase such that the baseband output can no longer be approximated as linearly proportional to the target displacement. The quadrature architecture has I/Q channels that are 90° out of phase. As a result, there is always one channel that is not at the null detection point, and thus avoiding the null detection point problem. Owing to the range correlation effect,¹⁵ the phase noise of the local oscillator is largely cancelled in the receiver baseband output in short-range sensing applications. Therefore, the first generation of radar sensor chips used free-running voltage controlled oscillator (VCO) but can still detect human vital signs when no phase locked loop is present. This largely reduced the overall system complexity and cost, and make single-chip solid-state realization of radar appealing for consumer electronics.

Because of the advancement of semiconductor process technologies, CW radar sensor circuits have shrunk to smaller and smaller size and the power consumption has been lowered over the past two decades. Many different versions of integrated radar chips have been reported. For example, besides the quadrature architecture, another architecture known for its double-sideband transmission was reported to avoid the null detection problem.²⁰ This is a type of heterodyne architecture without image band rejection. After mixing signals from the radio frequency (RF) local oscillator (LO) and the intermediate frequency (IF) local oscillator (LO), both the upper sideband and the lower sideband are transmitted, and the radar receives and processes the reflected signals of both sidebands by sequentially mixing them with the same RF LO and IF LO. It was demonstrated that the motion signals modulating both sidebands are automatically combined during this process. Therefore, the possibility of meeting a null detection point is significantly reduced. Furthermore, tuning the frequency of the IF LO can move the location of the remaining null detection points and thus avoid the null detection point problem for any given detection range. Fig. 2 shows a 5-GHz chip and its simplified block diagram with double-sideband architecture in 0.18 μm CMOS process.²¹ It integrated all the radio frequency building blocks so that the transmitter output can be directly transmitted to the target and the receiver output can be directly processed by baseband signal conditioning unit. Since the carrier frequency in 5-GHz band is higher than that of the first-generation radars in 1.6 and 2.4 GHz band, higher physiological signal modulation sensitivity were achieved.

As higher frequencies lead to higher detection sensitivity, recent efforts on CW radar sensor chip has moved into millimeter-wave range. In,²² a 90-nm CMOS process is used to implement a physiological radar sensor chip operating in 60-GHz band. In addition, the chip was integrated with the antennas into a system-in-package micro-radar solution based on flip-chip packaging. The radar chip uses heterodyne architecture with quadrature demodulation at 6-GHz

Figure 2. 5-GHz double-sideband radar chip. (a) Microphotograph. (b) Block diagram. [2013] IEEE. Reprinted, with permission, from Ref. 7.

Figure 3. (a) 60-GHz micro-radar system-in-package. (b) The radar chip microphotograph. [2013] IEEE. Reprinted, with permission, from Ref. 22.

intermediate frequency, and has 377 mW power consumption. Although the propagation of 60 GHz signal in air experiences high loss due to oxygen absorption, this unlicensed band is suitable for short-range physiological sensing and other applications such as material characterization. In lab experiments, the radar solution was able to detect a 20- μ m vibration at a 0.3 m distance, and detect a 0.2-mm vibration at a 2 m distance. It was also successfully used in human respiration and heartbeat detection,²² as well as heartrate monitoring of lab mice.⁶ Fig. 3 shows the chip microphotograph and the micro-radar system-in-package.

Other millimeter-wave radar-on-chip solutions have also been reported. For example,²³ reported a 60-GHz CMOS direct-conversion Doppler radar sensor chip with a clutter canceller for single-antenna noncontact human vital-signs detection. The chip was fabricated in 90-nm CMOS technology with a size of 2 mm $\times$ 2 mm and consumes a power of 217 mW. A high isolation quasi-circulator (QC) was designed to reduce leakage from the transmitter to the receiver. The clutter canceller cancels the transmitter-to-receiver direct coupling and the stationary clutter reflection, and thus can enhance the detection sensitivity of weak vital sign signals. The integration of the 60-GHz RF sensor consists of the voltage-controlled oscillator, divided-by-2 frequency divider, power amplifier, QC, clutter canceller, low-noise amplifier, in-phase/quadrature-phase sub-harmonic mixer, and three couplers. Connected a 17-dBi patch-array antenna, the chip was able to measure breathing and heart rate at a distance of 75 cm.

Moving toward higher frequencies, a 94 GHz CMOS Doppler transceiver-on-chip based on a double-sideband architecture was developed for remote monitoring of human respiration.²⁴ Because of attenuation and coupling, on-chip delivery of signals at such a high frequency is challenging. To avoid using a lossy LO tree, the 94-GHz transceiver chip uses a quadrature VCO that simultaneously produces four fundamental frequency signals in the 90–94 GHz band for LO signal distribution. It also features two power amplifiers (PAs) for potential beam steering. Each of the two PAs deliver a peak gain of 7 dB and saturated output power of 4 dBm. The chip has a size of 0.4 mm $\times$ 1.2 mm and draws 292 mW from 1.2-V DC supply. The receiver has a noise figure (NF) of 7–9 dB over a 17-GHz IF bandwidth. The chip was tested in lab environment to measure a target of 0.17 m² placed 1 to 3 m away and moving back and forth. Two horn antennas with 25-dBi gain were used for the transmitter and receiver, respectively. The system successfully measured Doppler shift signals from 30 to 300 Hz.

Beamforming technology for CW radar sensor chips.—In many sensing applications, it is desirable that the radar sensor chip can steer its beam to scan the space of interest. Intensive researches have been focused on developing the highly-integrated phased array in silicon-based technology in past decade.^{25,26} The potential applications target on the high-data-rate wireless communication and the sensing radars. Since the array can generate high-directivity beams, it not only improves the detection sensitivity due to the enhanced signal-to-noise ratio (SNR), but also nulls the unwanted interferers, making the radar

sensing link more secure. Furthermore, the array beamforming allows the radar to electronically steer the beam, making target search and tracking possible. To achieve array beamforming, the phase shifting can be done either in analog domain (RF path, IF path or BB path) or in digital domain. Each technology has different features but also has its own limitations. Within the existing RF-path beamforming techniques, Butler matrix (BM) has attracted intensive research over the years due to its unique properties, including low cost, zero power consumption, circuit simplicity, easy port impedance matching, high port-to-port isolation, and easy control. Furthermore, it can be directly adapted into readily developed RF transceivers without major changes on system configuration.

BMs are designed to generate a number of orthogonal beams from a linear array. By feeding the signal through different input ports, the corresponding phase distribution can be generated at the outputs to form a characteristic beam. A conventional BM is constructed by 3-dB quadrature couplers, phase shifters, and crossovers. Fig. 4 shows an example of a 4 $\times$ 4 BM and its corresponded phase distributions as well as beam direction. However, when it comes to monolithic integration, it becomes extremely challenging to implement those passive components due to the chip size limitation, especially for frequencies below 10 GHz. Although those passive components can be miniaturized using lumped elements instead of transmission lines, the consequent drawbacks include increased insertion loss and narrower operating bandwidth. In this review paper, three successful BM-based beamformer MMICs are briefly discussed, demonstrating their potential in 1-D/2-D radar sensing systems.

A significant progress of monolithic BM has been reported in Ref. 27, which was considered as the first demonstration of the BM MMIC in S-band. This 4 $\times$ 4 BM was designed at 2.5 GHz using TSMC 0.18- μ m CMOS technology. To overcome the size issue of those passive components, the transformer-based broadside coupler was proposed, as illustrated in Fig. 5a, where the inductive transformer is constructed by two fully-overlapped windings to acquire a strong mutual coupling. The key to this design is choosing an inductive coupling coefficient k greater than 0.707, so that transformer inductance as well as the chip area can be further reduced. This over-coupling mechanism also provides more design freedom to optimize the output balances, return losses, and port isolation.²⁸

Note that both windings are divided into two portions. One portion is routed on the Metal-6 (thick layer), and the rest of the portion is routed down to the vias-combined Metal-5/4 (thin layer). Such a geometric symmetry can ensure good phase/amplitude balance since each winding encounters the same trace length on each metal layer. The coupler itself was fabricated individually for further investigation, and the measured results demonstrate that phase balance is within $\pm 0.8^\circ$ and amplitude balance is less than ± 0.3 dB over a 10% fractional bandwidth.

Another essential component is the fixed 45°-phase shifters, which is commonly realized using two transmission lines with length difference. However, at 2.5 GHz, the required chip area appears impractical in CMOS implementation. Accordingly, reflection-type phase shifters

Figure 4. Block diagram of a 4×4 BM and the output phase distributions associated with beam direction. [2008] IEEE. Reprinted, with permission, from Ref. 27.

Figure 5. 2.5-GHz 4×4 BM, (a) schematic of the transformer-based quadrature coupler, (b) schematic of the phase shifter, (c) layout of the crossover, (d) chip photo. [2008] IEEE. Reprinted, with permission, from Ref. 27.

Figure 6. Photograph of the integrated switched-beam antenna array (left) and measured radiation patterns (right). [2008] IEEE. Reprinted, with permission, from Ref. 27.

(RTPS) is utilized in this work. The RTPS is composed of a quadrature coupler with Port-2 and Port-3 terminated by tunable accumulation-mode MOSFET varactors, in which the signals are reflected from those reactive loads with a relative phase shift. The tuning mechanism also provides the feasibility to compensate the phase errors due to the unpredictable fabrication variation. The insertion loss in RTPS design is critical, which is mainly caused by the loss of quadrature coupler due to the round-trip power flow. To reduce this loss, the edge-coupling instead of broadside coupling is employed in the transformer-based coupler design, where both windings are interleaved on thick Metal-6 layer to minimize the parasitic resistance, as shown in Fig. 5b. At 2.5 GHz, the simulated insertion loss and power imbalance is 1.6 dB and 0.5 dB, respectively. Within ± 1 V voltage bias, the simulated phase tuning range is approximated as 44° .

To create the signal crossover, one signal trace is kept on Metal-6 while the other trace is down to the combined Metal-4/3 through the vias, as shown in Fig. 5c. A grounded plane is placed on Metal-5 to shield both traces, further improving the isolation better than 50 dB according to the simulation prediction.

Fig. 5d shows the chip photo of the fully integrated 4×4 BM MMIC with chip size as $1.21 \times 1.25 \text{ mm}^2$, excluding the I/O pads. Within 2.4 to 2.6 GHz, the measured output amplitude imbalance is less than 1.2 dB fed from port-1 and less than 1.5 dB fed from

port 2. Except for the 6-dB distribution loss, the insertion loss is 4.5 dB, while the input return losses are better than 20 dB within 2.4–2.6 GHz. The relative phase differences activated by different feeding input are -135° (port-3), 45° (port-4), -45° (port-1), and 135° (port-2) with the phase error being less than $\pm 4^\circ$. To demonstrate its capability for beamforming, the chip is connected with a 1×4 monopole antenna array, as shown in Fig. 6. Four radiation beams are successfully generated in the directions of -45° (2L), -15° (1L), 15° (1R), and 45° (2R), respectively, with less than 1° beam direction error. Besides this work, it should be pointed out that the BM MMICs designed with different order or operating frequencies can be also found in other literatures.^{29–31}

There are numerous applications that require two-dimensional (2-D) radar coverage, such as air defense, surveillance, positioning or imaging. Accordingly, a phased array with 2-D beam scanning capability is essentially in need. A 2-D planar array also provides higher beam resolution with more symmetrical patterns, making it more versatile to use. A conventional BM can only achieve 1-D beam scanning. For 2-D beam scanning, it requires the double-stack configuration. Fig. 7a shows the example of a 16-beam configuration, in which four horizontally-stacked 4×4 BMs are used for elevation scanning, while the other four vertically-stacked 4×4 BMs are responsible for azimuth scanning.³³

Figure 7. 16-Beam BM-based beamformer for 2-D scanning. (a) double-stack configuration, (b) planar configuration. [2014] IEEE. Reprinted, with permission, from Ref. 32.

Figure 8. (a) Chip photo of 60-GHz, 16-Beam BM-based beamformer MMIC, (b) 2-D scanning radiation beams. [2014] IEEE. Reprinted, with permission, from Ref. 32.

A successful 2-D beamformer MMIC was reported in Ref. 32 by converting the double-stack configuration into a fully planar design. Fig. 7b shows the schematic of this 60-GHz 16-beam BM-based beamformer. Since it contains eight BMs, the circuit size becomes a critical issue, considering the amount of the components (32 quadrature hybrids, 16 phase shifters, 48 crossover and 32 interconnection lines). The broadside coupler³⁰ is thus employed to realize the 3-dB quadrature hybrids, where the coupling length is shortened from the conventional 0.25λ to 0.09λ using over-coupling mechanism, leading to a significant size reduction. Those BMs are carefully arranged and interconnected with 50- Ω microstrip lines to form the 16-beam beamformer. Fig. 8a shows the chip photo, which was fabricated using TSMC 0.18- μm CMOS process. The chip size is $2 \times 2 \text{ mm}^2$ including the I/O pads. Within 55–65 GHz, the measured progressive phase errors between adjacent outputs are less than 17° , and the average insertion loss of one signal path is 4.7 dB. Fig. 8b displays the calculated beam patterns based on the measured scattering parameters, showing that the resultant beams agree very well with theoretical predictions. The array gain ranges from 6.5 to 8.4 dB among those beam cases.

The order of the conventional BM determines the number of beams being generated in a certain spatial coverage. However, several radar applications, such as radar imaging or radar tracking, demand better beam resolution or continuously beam steering. A printed circuit board (PCB) realization of a 24 GHz radar with continuously beam steering capability has been reported in Ref. 34. Increasing the order of BM may enhance the beam resolution, but also leads to an impractically large chip area. Another beamforming approach is to use tunable phase shifters to generate the continuous beams, but it may also imply a great design challenge if a significant amount of phase tuning is required. In order to achieve a fine beam resolution, a 25-GHz low-power BM-based phased array receiver associated with the subsector beam steering (SBS) technique was proposed in Ref. 35. Fig. 9 shows the block diagram of this phased array receiver, which is composed of a conventional 4×4 BM followed by a beam steering network. It has been noticed that the radiation patterns can be further synthesized if two adjacent beams are excited simultaneously. With an appropriate combination of the amplitude and phase, continuous beam steering can be achieved. Based on this design concept, the so-called subsector beam steering technique divides the entire steering range into five subsectors. When a target RF signal is incident from an unknown direction, by sweeping each subsector with different weighted beam combinations, the target angle can be determined.

Based on the same design methodology of,²⁸ the 25-GHz CMOS BM was also designed using the over-coupled transformer. Simulations show that phase deviations are smaller than $\pm 5^\circ$ and isolation between antenna ports is larger than 20 dB. The beam steering network consists of two active selectors, two weighting factor controllers, and a signal combiner. The active selector, which is used to select and amplify RF signals from the BM, is composed of two gm-booster common-gate amplifiers and one cascoded amplifier, as shown in Fig. 10a. The common-gate amplifier can be biased either in the ON state to amplify the input RF signal or in the OFF state to block the signal, in which an embedded termination load is shunted at the input port to ensure good impedance matching in either state. The simulations predict 17-dB power gain, 4.7-dB noise figure, 23-dB isolation and 10-mW power consumption.

The weighting factor controller is a tunable attenuator associated with a switchable $0^\circ/180^\circ$ phase inverter, as shown in Fig. 10b. The reflection-type attenuator includes a quadrature coupler loaded with two MOSFET resistors (M1, M2), where the absorbed power level can be varied through the different gate bias. The phase inverter has a similar structure but both loaded MOSFETs (M3, M4) are simultaneously turned on or off to serve as short/open loads. The $0^\circ/180^\circ$ phase inversion can thus be accomplished. Note that the grounded inductors are added to the source nodes of M3 and M4 to moderate the phase deterioration due to the parasitic drain-body capacitance. This weighting factor controller can provide a weighting ratio from 0.1 to 0.9 according to simulations. The signal combiner, which has a cascaded structure as seen in Fig. 10c, performs a linear summation of two beams.

The entire receiver was fabricated using TSMC CMOS 0.13- μm technology, as shown in Fig. 11. The chip size is $1.3 \times 1.1 \text{ mm}^2$ with total power consumption of 30 mW with a 1.2-V supply. Within 25–26 GHz, the four-channel gain and noise figure are 17–21 dB and 8.9–10.7 dB, respectively. Based on the measured single-channel scattering parameters, Fig. 12 illustrates the calculated steering patterns under different weighted beam combination. Note that those patterns are normalized with respect to their own peak values to give a clear illustration on the change of beamwidth and nulls. The beam direction discrepancy is less than 2° comparing to the theoretical array patterns, which can be easily calibrated since the weighting factor in this work can be precisely adjusted. The subsector beam steering technique proposed in this work provides a simple and reliable method to enhance the functionality of the existing matrix-fed beamformer, leading to a

Figure 9. Circuit block diagram of the continuously-steering phased-array receiver with the divided subsectors. [2010] IEEE. Reprinted, with permission, from Ref. 35.

compact, low-power, continuously beam steering solution for radar sensing applications.

Baseband technology for CW radar sensor chips.—In order to increase the sensitivity of the radar detection systems, not only the carrier frequency was increased, but also different circuit architectures and digital signal processing (DSP) algorithms have been explored. Integration of variable gain amplifier (VGA) and analog-to-digital converter (ADC) with the radar systems into a single chip is presented in Ref. 36 to achieve clutter cancellation. The dc level of the baseband signal can be monitored and shifted to achieve the optimal dynamic range and thus improve the sensitivity of radar detection systems. Fig. 13 shows the system block diagram of a 5.8-GHz receiver for radar detection systems, where the direct-conversion architecture is employed. The reflection of radar CW signal from stationary objects has no phase modulations, and the mixing with local oscillator

will generate dc offsets and affect the baseband signal processing. Coupling effects inside the circuits may also cause clutter interferences. The clutter cancellation is placed after the mixer with dynamic dc level control in the VGA. By adjusting the dc level dynamically, the baseband signals can be kept within the optimum input range of the VGA. Since cardiopulmonary swing signals are in low-frequency band, flicker noise at low frequencies particularly affects the vital sign detections. In order to accurately restore the analog signals, the ADC is required to operate with high resolution. A 10-bit successive approximation register (SAR) ADC is integrated in the *I* and *Q* channels, respectively, to quantize the received signal. In this work, the circuits and systems were designed and fabricated in a TSMC 0.18 μm CMOS process technology.

The schematic of the VGA is shown in Fig. 14. Discrete-time switch-capacitor feedback operation is utilized in this design. Non-overlapping clock phases ϕ_1 and ϕ_2 control the switching circuits

Figure 10. Circuit schematic of the beam steering network, (a) active selector, (b) weighting factor controller, (c) signal combiner. [2010] IEEE. Reprinted, with permission, from Ref. 35.

of the VGA. In phase φ_1 , the input signal is sampled onto C_s , and then in phase φ_2 , the charge in C_s is fully transferred to the feedback capacitor C_f . When φ_2 is on, the capacitive feedback C_f is connected in parallel with the output impedance of the operational amplifier, which provides high impedance path and avoids reducing the closed-loop output impedance. The effective open-loop gain remains constant and the overall gain errors are reduced. Therefore, harmonic distortions can be minimized. The total capacitance in the sampling phase is controlled by the switched capacitor array to achieve the function of adjustable gains. The VGA provides a gain of 18–36 dB. Clutter cancellation is implemented in the VGA by tuning the reference voltage

V_{OA} . The dc level VGA output can be adjusted for cancellation of the dynamic clutter interferences. The detection of proper dc level is implemented with DAQ and Lab view tools. The differential outputs of the VGA were sent to the analog input port of the DAQ. The output dc level is processed by the 3-bit comparator in the dc Level detection module and the value of the dc level is converted into eight intervals. The 3-bit output codes are used for switching the 8-level multiplexer to generate the corresponding clutter cancellation voltage V_{OA} .

A single-ended input architecture is used in the realization of the ADC shown in Fig. 15. Because only one capacitor array is used, the area can be reduced by about 40% compared to the differential

Figure 11. Chip photograph of 25-GHz beam steering phased array receiver in 0.13- μ m CMOS. [2010] IEEE. Reprinted, with permission, from Ref. 35.

input architecture. The successive approximation register (SAR) ADC architecture mainly consists of a sample-and-hold circuit (S/H), a comparator, a digital-to-analog converter (DAC), and SAR logics. After the differential I/Q signal amplification by the VGA, the analog

Figure 13. The system block diagram of the physiological signal detection receiver in the cardiopulmonary detection radar system. [2016] IEEE. Reprinted, with permission, from Ref. 36.

buffer converts the differential signals into single-end outputs. Then, the SAR ADC converts the continuous analog voltages into discrete digital codes via the binary search algorithm. The sampled voltages are compared with a series of successively smaller voltages generated by the DAC. In each clock cycle, a single bit can be resolved. Using a single comparator, the monolithic ADCs achieve small die sizes and can operate with low supply voltages to reduce the power dissipation, making it an ideal candidate for on-chip biomedical applications. The implemented SAR ADC achieves a measured 8.6 effective number of bits (ENOB).

Fig. 16 shows the chip microphotograph of the RF front-end and the baseband circuits. The overall chip area is $4.15 \times 1.6 \text{ mm}^2$. The power consumption is about 55 mW from a single 1.8 V supply. The chip was tested for non-contact vital signs detection. Fig. 17 shows the vital sign transient waveforms without (top) and with (bottom) clutter

Figure 12. Calculated array patterns of steered beams based on the measured scattering parameters. [2010] IEEE. Reprinted, with permission, from Ref. 35.

Figure 14. The schematic of the baseband variable gain amplifier with clutter cancellation. [2016] IEEE. Reprinted, with permission, from Ref. 36.

Figure 15. The block diagram (left) and the layout (right) of the single-ended SAR ADC.

cancellation. It can be found that without clutter cancellation, there is a large dc offset voltage, approximately 1.6 V, at the output of the VGA, and the operational amplifiers are saturated. With clutter cancellation, the output DC level is maintained at about 0.9 V. The VGA outputs are connected with the on-chip ADCs for measurements. Because the radar chip has I/Q channels, the complex signal demodulation (CSD)

method was used for baseband signal processing. Fig. 18 shows the measured spectrum of the baseband vital sign signals detected from the back of a human subject. It can be seen from the spectrum that the subject's breathing was about 12 beats per minute, and heart rate was about 70 beats per minute. The second and third harmonics of the respiratory signal, caused by the nonlinear Doppler phase

Figure 16. The chip microphotograph. [2016] IEEE. Reprinted, with permission, from Ref. 36.

Figure 17. Measurement results of clutter cancellation.

demodulation in CSD, can also be observed from the measurement results.

UWB Radar Sensor Chips

In 2002, the Federal Communications Commission (FCC) authorized the marketing and operation of products incorporating ultra-wideband (UWB) technology³⁷ by modifying the 47 CFR Part 15 regulations.³⁸ UWB systems have been allocated in the unlicensed band of 7.5 GHz in the radio-frequency (RF) spectrum from 3.1 to 10.6 GHz. According to the FCC regulations, any devices operating in this frequency range and exploiting a bandwidth greater or equal to 500 MHz, or 20% fractional band, can be considered UWB devices. Similar regulations have been adopted also by other regulatory

bodies, e.g.^{39,40} Beyond these regulations, on the basis of the general definition, UWB device operations can be extended to other available unlicensed frequency bands at microwaves and mm-waves, such as the 24-GHz, 60-GHz and W bands, and potentially above.

UWB transceivers are conceived to transmit and receive extremely short radio-frequency pulses, with time duration in the range of hundreds of picoseconds to few nanoseconds. This was a key feature for radar applications, since very short pulses allow achieving very high spatial resolution. For the 3.1–10.6 band allocation above, the maximum Equivalent Isotropic Radiated Power (EIRP) spectral density allowed in band for UWB devices has been set to -41.3 dBm/MHz. Different out-of-band maximum levels are allowed in relation to the nature of the applications (medical, military, surveillance, etc.). New opportunities were envisaged for data communication, localization

Figure 18. Measured complex signal demodulated (CSD) spectrum of ADC output detected from the back of a human subject. [2016] IEEE. Reprinted, with permission, from Ref. 36.

and contactless systems for mass-market applications. As for radar systems, such as ground penetrating radars, wall and through wall imaging, surveillance, and medical imaging appeared as those of major interest. In particular, the combination of short pulses, i.e. high spatial resolution, with an extremely low power spectral density, has been very attractive for medical applications, where reduced interaction with human tissues is potentially an advantage with respect to narrowband Doppler radars.

However, the market penetration of the new class of UWB devices was strongly related to the opportunity of implementing ultra-miniaturized low-power low-cost solutions on standard silicon technologies. By coincidence, nano-scale CMOS technology was just to become the most advanced commercial technology for microelectronics industry. In particular, in those years matured the potential to support millimeter-wave operations,⁴¹ so enabling system-on-a-chip (SoC) implementation of low-cost radio transceivers, including radars, with all the required functionalities: communication, sensing and digital processing.

In spite of the potential of the nano-scale CMOS technology, the implementation of integrated pulse radars required a different design approach compared to traditional narrowband radio-frequency systems developed till then. The challenges were not limited to satisfy the ultra-wideband communication regulations, but, more than that, to design innovative architectures and building blocks such as pulse generator, antenna, etc. radically new with respect to those developed for the traditional narrow-band radio-frequency systems. New system architectures, circuit topologies, design methodologies were required to address effectively the challenges imposed by UWB radar system implementation. Most of them required the definition of new performance metrics, new simulation and measurement techniques. The international research community reacted very positively to those initial challenges and was very keen in addressing problems and prolific in anticipating solutions. A short summary of some relevant challenges addressed for UWB system implementations can be found in Ref. 42. In the next section, we report a short summary of the evolution and some major advances achieved to date by the international community.

UWB pulse radars: advances.—Pulse radars operate by sending short electromagnetic pulses and receiving the echoes reflected by the target. The time delay between transmitted pulse and received echo is given by the time of flight of the pulse, round trip from transmitter (TX), to the receiver (RX), which is therefore proportional to the distance from the radar to the target. Then, the target movements can be so detected. With respect to continuous wave (CW) radars, UWB pulse radar transceivers have a lower circuit complexity since no frequency synthesizers (typically, these are power-hungry blocks, which require anyway external frequency references provided by quartz crystals) for frequency conversions are required. This, together with a low pulse repetition frequency (f_{PR}), can lead to very low power consumption (P_C) and longer battery autonomy. Examples of pulse radars implemented by means of discrete components and applied to the detection of vital parameters are reported in literature.^{43–45} Hereinafter we report a summary of some of the most representative developments of integrated radar systems on silicon, along with a short description and their main features and targeted applications, with the objective to provide an overview of the diverse solutions reported in the literature. From this, it comes out that these solutions can be classified in two main categories: *analog correlation-based* and *digital direct-sampling* radars. As per intentions, we will focus on SoC solutions, rather than multi-module solutions. Whether available, further details related to their operation, design and measurement results can be found in the original references.

Analog correlation-based UWB pulse radar.—In Ref. 46, Zito et al., reported the SoC CMOS implementation of a UWB pulse radar for based on a correlation receiver. The solution is compliant with the FCC spectrum mask regulations and allows motion detection, in particular respiratory rate monitoring. Block diagram and operating principle are highlighted in Fig. 19.

Figure 19. a) Block diagram of the SoC UWB pulse radar. The dashed lines around the target indicate the spatial range spanned by the radar. b) Representation of the pulses at the input and output of the multiplier for three different cases of relative shift (δ) between the input pulses. c) Representation of the input and output voltages of the integrator for static and moving targets. [2011] IEEE. Reprinted, with permission, from Ref. 47.

The pulse generator (PG) transmits short pulses toward the target (i.e. human body) with a pulse repetition frequency (f_{PR}). The signals reflected by the target are captured by the RX antenna, amplified by the LNA and correlated (multiplied and integrated) with a delayed replica of the transmitted pulses generated on-chip by the shaper. The signal at the output of the multiplier is integrated in order to increase the signal-to-noise ratio (SNR) and capture the envelope containing the information on the movement rate. The integrator is implemented by means of a low-pass filter with bandwidth B in the order of 100 Hz. Averaging a large number of pulses (in the order of f_{PR}/B) allows increasing the SNR_{out} . The operating principle can be explained intuitively as follows. For simplicity, let us assume that the delay generator (DG) provides a delay equal to the entire time-of-flight (round trip) of the transmitted and received pulses. In principle, if the target is static, the local replica and the amplified echo are aligned in time and the multiplier provides the same output pulse with a pulse repetition frequency f_{PR} , as shown in Fig. 19b, case (a). Therefore, the signal at the output of the integrator is quite constant, as shown in Fig. 19c. Note that, in principle, the integrator will provide a constant output voltage regardless of the relative shift (δ) between the local replica and amplified echo, for any other constant δ . If the target is moving, the movement causes a time-varying δ between the local replica and the echo amplified by the LNA. Therefore, the multiplier provides an output pulse that may be positive, negative or zero, depending on the δ caused by the time-varying distance between

radar and target, due to the target movements around its quiescent position.

The radar sensor is thought to operate in two operating modes: ranging mode (RM) and tracking mode (TM). In RM the DG provides a variable delay in order to span the spatial (time) range of interest and identify the target (see Fig. 19a). In RM the radar sensor allows identifying the presence of the target and the time of flight. When the target is detected, the radar can switch to the TM, in which the DG provides a fixed delay (i.e. equal to the time of flight identified in RM) in order to monitor a fixed range gate (see Fig. 19a). Therefore, the output voltage is directly sensitive to the target movements, e.g. the chest movement due to the pulmonary activity in case of respiratory rate monitoring. The output voltage can be expressed approximately as follows:

$$\begin{aligned} v_{OUT}(t) &= A \frac{B}{2\pi} \int_{t-\frac{2\pi}{B}}^t v_Q(\tau) \times v_P(\tau) d\tau \\ &= A \frac{B}{2\pi} \int_{t-\frac{2\pi}{B}}^t v_Q(\tau) \times v_Q(\tau - \delta) d\tau \end{aligned} \quad [1]$$

which is obtained assuming that the amplified echo has the same shape of the transmitted pulse (i.e. the same of the local replica), but different amplitude (α is the attenuation factor, A is the correlation gain, B is the bandwidth of the low-pass filter and δ the relative delay between the input signals of the multiplier). It is important noticing that the information is now in a low-frequency signal, which can be sampled very conveniently by means of ADC with very low sampling rate, reduced circuit complexity and very low power consumption. Note that the relation time-space between transmitted pulses and received echo allows filtering out unwanted reflections and interferers, so contributing to mitigating signal-to-noise degradation in the receiver.

Excluding the low-pass filter, all building blocks such as pulse generator, low noise amplifier and multiplier have been implemented by introducing innovative circuit topologies specifically thought to meet the radar system requirements. In the actual implementation, the shaper is realized by using the same design principle of pulse generator. The pulse generator provides monocycle pulses with a 350-ps duration time and about 900-mV peak-to-peak voltage. The power spectral density is relevant in the frequency band 3–5 GHz. Details about the design challenges and implementation of the building blocks, radar microchip, planar TX and RX antennas, and their integration for the realization of the overall radar sensor are reported in Ref. 48–50.

The radar microchip has been implemented in a 90-nm bulk CMOS technology. This is shown in Fig. 20. The microchip area amounts to about 2 mm² and power consumption to about 73.8 mW from a 1.2-V supply. The operational tests carried out within a distance radar-target within one meter have shown the detection of sub-centimeter spatial resolution and respiratory rate patterns in adults (both genders) and infant volunteers, including apnoea. These results have been obtained by means of a compact radar sensor with novel low-cost planar antennas,^{48–50} as shown in Fig. 21, without adopting complex and

Figure 20. Radar microchip. a) silicon die; b) packaged chip. [2011] IEEE. Reprinted, with permission, from Ref. 47.

Figure 21. Radar sensor with packaged microchip and TX/RX planar differential antennas. Size: 12 cm × 10 cm. [2014] IEEE. Reprinted, with permission, from Ref. 50.

bulky three-dimensional structure antennas more directive and with superior performances. The results of a large variety of in-vitro and in-vivo tests are reported in^{47,51}

Digital direct sampling-based UWB pulse radars.—The analog correlation adopted in the radar transceiver architecture above can be replaced by direct digital sampling of the received signal available at the output of the LNA. This is the principle behind digital direct sampling pulse radars, whose general architecture is shown in Fig. 22.

The digital sampling time must be related to the pulse transmission time in order to determine the time of flight and the distance radar-target. Thereby, direct sampling radar architecture do not require a local replica of the transmitted pulse. These features result in a higher flexibility, but direct sampling of narrow pulses requires fast sampling and thereby analog-to-digital converter (ADC), and also some level of parallelism in acquiring and processing signal samples. Fast sampling and fast ADCs may lead to unsustainably-high power consumption, unless special circuit and processing techniques are applied to relax the constraints on sampling rate and reduce digital processing. Sampling operation requires also anti-aliasing filters, which can be offered by LNA and RX antenna selective frequency responses. Time-space filtering is operated by sampling in correspondence of the time of flight of the desired echoes, in a similar way as for the delay control of the local replica in analog correlation-based receiver of Fig. 19a.

As an example, in Ref. 52, Chu et al., proposed a solution exploiting the quasi-stationarity of the target still for human motion detection, in which a 16-way analog processing unit is adopted to mitigate the

Figure 22. General architecture for digital direct sampling-based UWB pulse radars. The analog interface has typically some level of parallelism so allowing adequate processing capability of sampled signals, and driving capability of the ADC (not shown). Despite depicted as differential in analogy with the block diagram for analog correlation-based radars, antennas can be either differential or single ended.

Figure 23. Radar microchip in Ref. 52. [2011] IEEE. Reprinted, with permission, from Ref. 52.

high power consumption due to wideband direct sampling. The radar microchip has been implemented in a 130-nm CMOS technology and has an area of about 12 mm². The die photograph is shown in Fig. 23. The overall radar sensor includes a number of off-chip blocks, including ADC, TX and RX antennas. However, the power consumption of the proposed solution, i.e. about 695 mW, was still considerably high.

In Ref. 53, Park et al., reported a single-chip impulse radar transceiver with a 100-ps resolution four-channel sampling receiver, for in/outdoor human walk tracing, stride-rate and respiration measurements. In order to relax the sampling rate, periodic pulses are transmitted so allowing an equivalent sampling time corresponding to the time difference between the pulse repetition interval and the sampling period. The proposed radar architecture includes also a transmitter with adjustable frequency spectrum, which introduce an additional degree of flexibility on pulse width and central frequency in the band 3–5 GHz. Despite the good level of integration including transmitter, TX and RX digital clock signal generator and embedded controller, four-channel track and hold sampler and integrator, and LNA, the radar sensor prototype requires some extra off-chip components, such as additional LNA, four-channel ADC, control and signal processing unit and external frequency reference, and TX and RX antennas. The single-chip radar module has been implemented in a 130 nm CMOS technology. The microchip area is about 3 mm² and the power consumption of the entire transceiver amounts to about 103.2 mW. The maximum resolution amounts to 1.5 cm. For operational tests, the radar transceiver chip was integrated into a board-level radar sensor system as shown in Fig. 24. The results of the operational tests carried at about one-meter distance show the detection of the volunteer's respiration rate.

In Ref. 54, Kao et al., reported a direct-sampling pulsed radar with digital-to-time converter (DTC) for estimating the time of flight. The adoption of a DTC allows performing equivalent-time sampling, so alleviating the sampling-rate and consequently the power consumption. In particular, it adopts a frequency-defined Vernier DTC, which allows higher time resolution, so increasing the spatial resolution. The time difference ΔT is defined by start and stop edges of two synchronized oscillations generated by two phase locked loops derived by the same frequency reference. The microchip radar includes pulse generator together with delay generator and edge combiner in the transmitter chain, DTC, digital control circuit, and LNA, variable gain amplifier (VGA), programmable gain amplifier (PGA), sample and hold and baseband circuit including low-pass filter and ADC, in the receive chain. The overall radar sensor includes off-chip frequency reference, hybrid TX driver amplifier, microwave hybrid coupler, and TX and RX horn antennas.

Figure 24. Radar sensor with microchip and board in Ref. 53. [2014] IEEE. Reprinted, with permission, from Ref. 53.

Figure 25. Radar microchip in Ref. 54. [2015] IEEE. Reprinted, with permission, from Ref. 54.

The radar microchip has been fabricated in a 65-nm CMOS technology and occupies an area of about 2 mm². The microchip in shown in Fig. 25. The power consumption amounts to about 88.2 mW. The results of the lab tests show the detection of back and forth movements of a metal plate of 30 × 30 cm²; however, details about distance and spatial resolution are not reported therein.

In Ref. 55, Wang et al., proposed a radar transceiver with single antenna and diplexer for the detection of respiratory patterns. The radar microchip has been implemented in a 130-nm CMOS technology and has an area of about 2 mm². The overall radar sensor includes a number of off-chip blocks, such TX/RX antenna and ADC. The power consumption amounts to 20 mW from a 1.2-V supply. The radar sensor and microchip are shown in Fig. 26. The measurement results show the detection of breathing rate up to a distance radar-target of 50 cm.

Figure 26. Radar sensor with microchip and board in Ref. 55.

Figure 27. Die photograph of the radar microchip in Ref. 56. [2017] IEEE. Reprinted, with permission, from Ref. 56.

In Ref. 56, Andersen et al., reported a direct-RF pulse-based system-on-chip UWB pulse radar with applications in vital sign monitoring and occupancy detection. The proposed solution is compliant with FCC and other regulation masks. In order to mitigate the issues related to the high power consumption and circuit complexity, the proposed solution adopts a swept-threshold (ST) digital sampling technique, whose operating principle can be explained as follows. In relation to the pulse transmission, after a certain delay that depends on the time of flight, a trigger signal is made available to the receiver. There, after such a time, the received pulse is compared with a threshold voltage that is kept constant for the entire duration of the received pulse. The comparison with the constant threshold produces a one-bit digitalized signal. When the received signal is above the threshold, the output of the comparator will increment the counter in correspondence of the trigger signal. Otherwise, no increment in the counter. By repeating this operation several times and, at each time, stepping the threshold voltage all through a discrete set of values of the dynamic range of the received signal, the number of the counts in the number of sampling time intervals will allow estimating the input signal, as these approximate its cumulative distribution. Thereby, this technique allows some tradeoff between sweep time and processing, depending on the location of the radar sensor and distance from the target, as well as the presence of interferers due to close reflective objects.

The transmitter adopts a direct-RF synthesis of frequency-shifted Gaussian-like pulses with programmable pulse repetition frequency, output power, polarity and central frequency, with relevant spectrum in bands of about 1.5 GHz around 7.29 and 8.75 GHz set by internal PLL operations. The receiver includes high-pass filter, LNA, pre-amplifiers, comparators, digital-to-analog converter (DAC) used to set the threshold step values and serial-to-parallel interface. The overall radar sensor includes off-chip frequency reference, and TX and RX antennas (not specified). The receiver samples the input signal received by the antenna and amplified by the LNA at a sampling rate of about 23.38 GS/s.

The radar microchip has been implemented in a 55-nm CMOS technology. The microchip is shown in Fig. 27. It includes also power management and control logic units. The power consumption amounts to about 118 mW from a 1.8-V supply, in transmit and receive mode without duty cycling. After some post-processing, measurement results show breathing profile and heartbeat plots from volunteer facing the radar sensor at a distance of about 5 and 9 m.

In Ref. 57, Park et al., reported a single-chip pulse radar transceiver with continuous sweep-clock generator, spectrum adjustable transmitter and wideband sampling receiver, for breathing motion detection.

Figure 28. Layout and radar microchip in Ref. 57. [2018] IEEE. Reprinted, with permission, from Ref. 57.

The proposed solution makes use of a so called time-expansion technique exploiting the quasi-stationarity of the target in the specific application. The operating principle can be summarized as follows. Two clock signals are generated from a clock generator block comprising a delay generator: the clock signal to trigger the TX and the clock signal, with a controlled delay with respect to the former, to drive the track-and-hold sampler (TSH) at the output of the integrated LNA. When the TX is triggered by the clock signal, it sends out pulses through the antenna. After a delay, i.e. TX-to-RX clock delay, related to the time of flight, the RX clock signal samples the received signal. To span a certain range, multiple pulses are transmitted and each of them are sampled at different times, with different TX-to-RX clock delay swept linearly by means of a command voltage. By considering quasi-static targets, the profile of an echo signal could be reconstructed piece by piece from multiple received pulses, over an expanded time scale.

The microchip radar includes the clock generator block; LNA, TSH and integrator in the receiver chain; and a voltage-controlled ring oscillator (VCRO) with control circuitry in the transmitter chain. Layout and microchip are shown in Fig. 28. The transmitter provides signals with 500 MHz with central frequency between 0.5–1 GHz. Thereby it operates outside the 3.1–10.6 GHz UWB range and output spectrum measurements show lack of compliance with FCC spectrum mask, so appearing these as significant limitations. The overall radar sensor includes also off-chip frequency reference, TX filter, RX and TX horn antennas, and additional LNA. The radar microchip has been fabricated in 130 nm CMOS technology and has an area of about 1 mm². The power consumption amounts to about 30 mW. The results of the lab tests report the detection of back and forth movements of a metal plate of 10 × 10 cm², for a resolution of 2.5 mm at a distance of 1.2 m.

Summary for UWB pulse radars.—This section has summarized in short the main characteristics of the UWB pulse radio technology, as well as some of the most significant challenges and most representative advances toward system-on-chip UWB pulse radars. The solutions reported in the literature can be classified in two main categories: analog correlation-based and digital direct-sampling radars. Analog correlation does not suffer from the high power consumption associated with high-rate digital sampling, which offers the potential for a higher flexibility. A number of techniques have been proposed to mitigate the high power consumption associated with direct sampling solutions. A direct comparison between solutions is not entirely feasible for a number of reasons, such as some missing details in the original reference, diversity of operation bands, operating scenarios and measurement setups. But, above all, the adoption of different antennas with sensibly different performance, form and cost factors do not allow a direct and fair comparison between proposed microchip radar solutions. Anyway, the comparison is beyond the intentions of this short survey. The most important aspect emerging from this investigation is that substantial progresses have been made to date in terms of advanced solutions to technical challenges and system-on-chip integration, with respect to the hybrid solutions reported about ten and more years. In

achieving such important advances, particularly important have been: (a) the initiative driven by FCC in regulating and authorizing the marketing and operation of ultra-wideband (UWB) technology; (b) the significant advances of silicon technology, in particular CMOS; (c) and the outstanding reaction and enthusiasm manifested by the international research community. Designers, mostly from academia and spin-off/start-up companies, have been tackling the new challenges imposed by UWB operations, all levels: theory, modeling, design, simulation and experimental characterization. A good number of innovative integrated circuit and system solutions have been proposed for effective system-on-chip UWB pulse radars, so making up the large deficit in terms of building blocks and design methodologies and techniques compared to those already well-established for narrowband applications.

Commercial Applications and Outlook

As highly integrated radar systems become an important technology for healthcare monitoring, internet of things (IoT) solutions, drone navigation assistance, and self-driving driving cars, the semiconductor industry are providing radar-on-chip solutions targeting various consumer markets. For example, Texas Instruments (TI) provides the AWR1642 single-chip, which is a self-contained FMCW radar sensor single-chip solution for automotive radar sensors in the millimeter-wave frequency band of 76 to 81 GHz. The chip is fabricated in TI's low-power 45-nm RFCMOS process, which enables a monolithic implementation of a 2-transmit-channel, 4-receive-channel system with built-in PLL and analog-to-digital converters. It integrates TI's high performance C674x DSP for radar signal processing. The device includes an ARM R4F-based processor subsystem responsible for radio configuration, control, and calibration. TI also provides a low-cost evaluation board which serves as a complete system configuration reference. In addition to automotive radar sensor ship, TI provides the IWR1443 single-chip solution, which is a 76-to-81GHz FMCW radar sensor chip also fabricated in TI's 45-nm RFCMOS process. This chip features 3 transmit-channels and 4 receiver-channels with built-in PLL and analog-to-digital converters. It includes hardware accelerator that supports complex FFT and constant false alarm rate CFAR detection. Additionally, it has two ARM R4F-based processor subsystems for two purposes: master control with additional algorithms, and front-end configuration, control, and calibration. The IWR1443 chip is targeted for low-power, self-monitored, ultra-accurate industrial applications such as drones, factory automation, building automation, material handling, traffic monitoring, and surveillance. Analog Devices has radar-on-chip solutions in the 24-GHz and 77-GHz bands, featuring advanced beamforming capabilities for automotive applications. The 24-GHz chip was also demonstrated for noncontact vital signs monitoring in the exhibition of the 2017 IEEE International Microwave Symposium. Infineon Semiconductors have radar sensor chips operating in the 60-GHz band, and has demonstrated remote gesture recognition and control of tablets.

Not only large semiconductor corporations, but new companies are also pushing hard in commercializing radar sensor chips to improve the quality of life. For example, Novelda AS in Norway specializes in low-power technology for ultra-high resolution impulse radar. Their XeThru Impulse Radar is a complete single-chip CMOS radar system that can be used to implement a high-precision electromagnetic sensor for human vital sign monitoring, personal security, environmental monitoring, industrial/home automation and other novel sensor applications.

Empowered by the rapid advancement of solid state science and technologies, as well as modern embedded signal processing methods, it is expected that more research and commercialization activities will take place in this exciting field of radar system integrated on chip. It is envisioned that in the future, radar chips could be as popular as other semiconductor devices used in people's daily life routines.

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