Feasibility study of integrated photonic oscillators with 5 fs timing jitter

(Student paper)

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ABSTRACT

A time-domain circuit simulation of a photonic integrated circuit (PIC)-based optoelectronic oscillator (OEO) is presented. The implementation on-chip poses changes to both the modelling method and the performance metrics of such an integrated OEO. Noise from spontaneous emission, as well as optical filters are considered and related to the phase stability of the OEO. A design study reveal that performance beyond state of the art electronic oscillators is feasible from PIC based OEO's with current commercially available integration platforms, showing timing jitter of 5 fs @ 10kHz-10MHz offset frequency for 20-GHz oscillators.

Keywords: Optoelectronic Oscillator, Photonic Integration, Circuit Simulation, Phase Noise

1 INTRODUCTION

Well defined oscillations are a central part in modern technology. They provide the clock frequency for computing systems, enable carriers for information in wireless communication and provide timing in GPS and radar systems. The optoelectronic oscillator (OEO), realised for the first time 20 years ago[1], offers performance in the GHz-regime significantly beyond what can be achieved by other oscillator types, such as crystal-based oscillators. This paper investigates the feasibility of integrating the OEO on a photonic integrated circuit (PIC), with respect to phase stability. For an oscillator the prime concern is phase stability, measured either as a phase noise spectrum or as a timing jitter in a given offset frequency range.

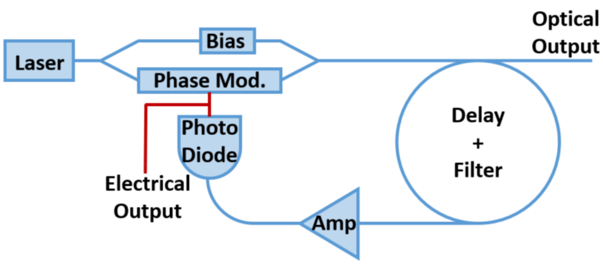

Figure 1. The proposed layout for a PIC based OEO. Note that although no electrical parts are needed in the oscillator loop the laser and amplifier still needs a driving current while the modulator and photo-diode need an applied bias.

The layout of an OEO realized with purely optical components can be seen in Fig. 1. This layout differs from the typical OEO[1] primarily from the fact that amplification and filtering in the present case is done optically, instead of electrically. The delay is traditionally realized in optical fiber, whereas an integrated OEO can utilize on-chip spiral delay or high Q resonant structures. In order to assess the performance realizable with PIC's and for design considerations a flexible and realistic simulation tool is required.

2 SIMULATIONS

Various efforts have been made throughout the years to model the phase noise of OEO's. With the invention of the OEO a simple analytic model relating the oscillator to the linear Leeson model was initially presented[1]. Since then several analytic and numeric implementations have been presented with varying flexibility and accuracy, among them a time domain phasor propagation model presented in [2] which is the framework our current work is based upon. The key to this model is to separate the fast time-scales of the light-carrier and oscillation frequency from that of the round-trip time. In doing so one can simulate the oscillator loop for thousands of round trips within a reasonable computation time. Within each round-trip appropriate functions are multiplied to the phasor, modelling the transfer through modulator, amplifier, photo-diode (PD), etc, as shown in Fig. 1. For each round-trip the signal is stored and finally the combined phase-vector of the simulation period is Fourier transformed to give the phase noise[2].

Working on the basis of [2], a model tailored for chip-scale oscillators has been developed. Since propagation losses are significantly higher for on-chip waveguides compared to optical fibers, propagation loss has been included. Furthermore saturation limitations have been included for the amplifier and the photo-diode to allow for a realistic relation to the well-known specifications offered by multi-project wafer (MPW)-based PIC fabrication.

The transition to all-photonic oscillators introduces the need for modelling optical filters and amplifiers. The noise in the semiconductor optical amplifiers (SOA's) is assumed dominated by amplified spontanous emission (ASE) and is modelled as a white noise power given by[3]:

$$P_{ASE} = \frac{hc}{\lambda_c}\beta_{eff}BN^2\sigma L_{SOA}, \tag{1}$$

where $\lambda_c = 1550nm$ is the centre frequency of the gain medium, β_{eff} the coupling factor to the optical mode, BN^2 the recombination due to spontaneous emission, σ the cross section of the active region and L_{SOA} is the length of the amplifier. Values for β_{eff} and BN^2 differ quite significantly between publications. In Fig. 2, the phase noise spectrum is compared for OEO's with electrical amplification and optical amplification, with parameters taken from [4] and [5]. Here it can be seen that the use of an optical amplifier leads to a decrease of 13 and 30 dB in the phase noise, as compared to an electrical amplifier.

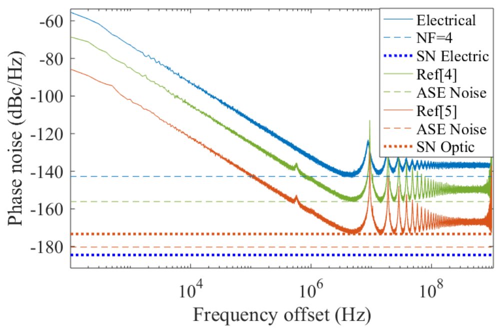

Figure 2. OEO phase-noise simulated with electrical amplifier (blue) and SOA amplifier (green and red). The white noise contributions from shot noise and chosen amplifier are plotted along with the phase noise spectrum. Note that the two simulations with optical amplification share shot noise value.

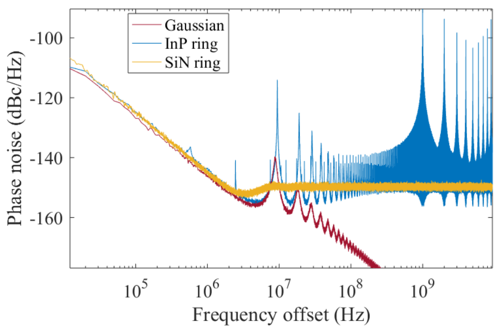

Figure 3. Phase noise spectra of an OEO for varying filter functions and all other parameters equal. The variations are an electrical gauss-passband (red), a InP ring resonator (blue) and a SiN ring resonator (yellow). The spurious peaks are matching with the round-trip time of the OEO.

Optical filters have been included in the model as a ring resonator response function. The filter is applied as a perfect filter with no loss since the delay is kept as a linear propagation with loss for ease of implementation. In realizations of a PIC-based OEO one would likely use a ring resonator as both delay and filter, and an implementation reflecting this will be studied in future. Filters considered for this paper is state of the art ring resonators from the silicon nitride (SiN) platform (FSR=3.3GHz and FWHM=3.2MHz [6]) and the indium phosphide (InP) platform (FSR=1GHz and FWHM =160MHz [7]). For comparison a Gaussian passband filter (FWHM=20MHz) applied in the electrical domain is considered as-well. A plot of the impact on phase noise from the three filters can be seen in Fig. 3, which shows that the SiN ring effectively cancel the spurious peaks while the InP has problems suppressing the peaks at frequencies near its FSR.

3 DESIGN CONSIDERATIONS AND PERFORMANCE

The prospect of having an OEO on a chip leads to a number of new design-considerations. First of all the propagation loss in the delay line is much higher leading to shorter delays, but also to an increased importance of amplifier noise. The longest delays currently achievable on chip is found on the SiN platform with resonant rings achieving equivalent lengths of >25 m [6]. In order to combine the active performance of the InP and the high-Q elements of SiN hybrid integration would be well suited in a realization of a chip-scale oscillator. Using SOA noise parameters from [4], [5] and fixed values for laser-power, PD and amplifier performance the timing jitter and corresponding noise contributions is plotted against delay length, as shown in Fig. 4. It is evident that for a certain length the SOA-noise becomes dominant and cancels the performance gain from increasing the loop length. The two figures further show that this optimized length vary not only with noise power but also with the frequency offset interval specifying the timing jitter.

Another possibility that arises with photonic integration is the ability to parallelize certain sections of the OEO. Typically optical phase-modulators require quite high driving voltage (>5V) and due to the absence of electrical amplification the PD needs to drive the modulator directly. It is, however possible to increase the power handling capabilities of this link by parallelizing the amplifier and PD section as seen in Fig. 5. Simulation results of this parallel approach are shown in table 1. Device specifications are chosen in accordance to claimed values from MPW runs on the InP platform[8] with ASE-parameters from [4] while only the amplification and laser-power are adjustable parameters (for reference it should be noted that the device specifications up until this point has been chosen as slightly higher than current MPW-specs). The simulations where performed by setting the laser input as high as possible while maintaining stable oscillation (limited by the PD) and subsequently

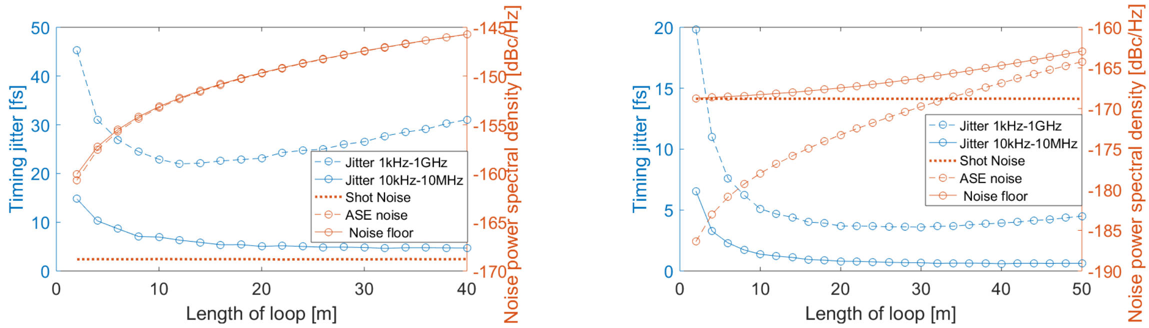

Figure 4. Timing jitter (in fs) as a function of delay length (left axis) and the corresponding noise contributions (right axis). The figure to the left is with ASE-parameters from [4] and the right with ASE-parameters from [5]. Note the difference in scale and range of the axes.

lower the amplification to the threshold of steady-state unity gain. From the simulations summarized in table 1 it is clear that with current performance, a single PD cannot drive the modulator to sufficient depth as it is unable to generate a signal stronger than the system noise floor. For an increasing number of lines an improvement in phase stability of the OEO is seen, achieving timing jitter of 5 fs in a 10kHz-10MHz offset frequency range. However it is also evident that too high power in the oscillator results in performance degradation. This is due to over-saturation of the amplifier as well as the output voltage from the PD-array exceeding the V_π of the modulator. This upper limit is however somewhat theoretical as the input laser powers become inflated and unrealistic, the phase modulator could simply be designed shorter raising the V_π while decreasing the loss.

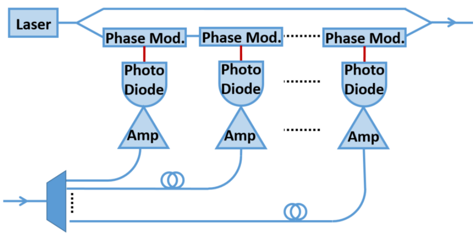

TABLE 1. PARALLELIZATION OF AMPLIFIER AND PD

Amp +PD lines	Input		Output		
	P_{in} [mW]	*Amp. gain* [dB]	P_{osc} [dBm]	*Jitter* [fs] 1kHz-1GHz	*Jitter* [fs] 10 kHz-10MHz
1	——– PD limited ——–				
2	13.7	14.73	5.688	27.02	9.643
4	45.1	12.49	15.06	15.11	5.312
8	92.4	12.17	20.30	13.39	4.727

Figure 5. Design proposal for distribution of optical power over multiple lines of amplification and detection. For high-speed operations the phase of the input channels should be matched to the propagation speed of the signal being modulated. The higher power handling of the link results in better oscillator performance as seen in table 1.

4 ACKNOWLEDGMENT

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5 CONCLUSION

With the presented simulation model the performance of chip-scale OEO's has been evaluated. According to [9] state of the art electronic oscillators offer 100 fs timing jitter from 10kHz to 10 MHz while the photonic oscillators presented in the same publication can provide 10 fs timing jitter in the same range. The performance capabilities expected from chip based OEO's goes beyond this metric promising 5 fs jitter which in turn for instance will enable high-bandwidth ADC's for use in radar systems[9]. Along with the performance gain the realization of chip-based OEO's will improve size, weight and power (SWaP) metrics significantly as previous photonic oscillators have been based on box-lasers and fiber spools.

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